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MOTOROLA

MC1495

Wideband Linear Four-Quadrant Multiplier

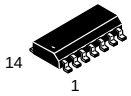
The MC1495 is designed for use where the output is a linear product of two input voltages. Maximum versatility is assured by allowing the user to select the level shift method. Typical applications include: multiply, divide*, square root*, mean square*, phase detector, frequency doubler, balanced modulator/demodulator, and electronic gain control.

- Wide Bandwidth
- Excellent Linearity:
  2% max Error on X Input, 4% max Error on Y Input Over Temperature
  1% max Error on X Input, 2% max Error on Y Input at + 25°C
- Adjustable Scale Factor, K
- Excellent Temperature Stability
- Wide Input Voltage Range: ± 10 V
- ±15 V Operation

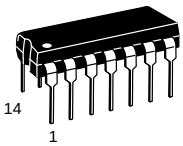
*When used with an operational amplifier.

LINEAR FOUR-QUADRANT MULTIPLIER

SEMICONDUCTOR TECHNICAL DATA



D SUFFIX
PLASTIC PACKAGE
CASE 751A
(SO-14)



P SUFFIX
PLASTIC PACKAGE
CASE 646

MAXIMUM RATINGS (T_A = + 25°C, unless otherwise noted.)

Rating	Symbol	Value	Unit
Applied Voltage (V_2–V_1, V_{14}–V_1, V_1–V_9, V_1–V_{12}, V_1–V_4, V_1–V_8, V_{12}–V_7, V_9–V_7, V_8–V_7, V_4–V_7)	ΔV	30	Vdc
Differential Input Signal	V_{12}–V_9 V_4–V_8	± (6+I_{13} R_X) ± (6+I_3 R_Y)	Vdc
Maximum Bias Current	I_3 I_{13}	10 10	mA
Operating Temperature Range MC1495 MC1495B	T_A	 0 to +70 – 40 to +125	°C
Storage Temperature Range	T_{stg}	– 65 to +150	°C

ORDERING INFORMATION

Device	Tested Operating Temperature Range	Package
MC1495D	T_A = 0° to + 70°C	SO–14
MC1495P		Plastic DIP
MC1495BP	T_A = – 40° to +125°C	Plastic DIP

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Rev 0

ELECTRICAL CHARACTERISTICS (+V = + 32 V , –V = –15 V, T_A = + 25°C, $I_3 = I_{13}$ = 1.0 mA, $R_X = R_Y$ = 15 kΩ, R_L = 11 kΩ, unless otherwise noted.)

Characteristics	Figure	Symbol	Min	Typ	Max	Unit
Linearity (Output Error in percent of full scale)	5					%
T_A = + 25°C						
–10 < V_X < +10 (V_Y = ±10 V)		E_{RX}	–	±1.0	±1.0	
–10 < V_Y < +10 (V_X = ±10 V)		E_{RY}	–	± 2.0	± 2.0	
$T_A = T_{Low}$ to T_{High}						
–10 < V_X < +10 (V_Y = ±10 V)		E_{RX}	–	±1.5	± 2.0	
–10 < V_Y < +10 (V_X = ±10 V)		E_{RY}	–	± 3.0	± 4.0	
Square Mode Error (Accuracy in percent of full scale after Offset and Scale Factor adjustment)	5	E_{SQ}				%
T_A = + 25°C			–	± 0.75	–	
$T_A = T_{Low}$ to T_{High}			–	±1.0	–	
Scale Factor (Adjustable) $\left(K = \frac{2R_L}{1_3 R_X R_Y}\right)$	–	K	–	0.1	–	
Input Resistance (f = 20 Hz)	7	R_{inX}	–	30	–	MΩ
		R_{inY}	–	20	–	
Differential Output Resistance (f = 20 Hz)	8	R_O	–	300	–	kΩ
Input Bias Current	6					µA
$I_{bx} = \frac{(I_9 + I_{12})}{2}$, $I_{by} = \frac{(I_4 + I_8)}{2}$ T_A = + 25°C		I_{bx}, I_{by}	–	2.0	8.0	
$T_A = T_{Low}$ to T_{High}			–	2.0	12	
Input Offset Current	6					µA
$\lvert I_9 - I_{12}\rvert$ T_A = + 25°C		$\lvert I_{iox}\rvert$, $\lvert I_{ioy}\rvert$	–	0.4	1.0	
$\lvert I_4 - I_8\rvert$ $T_A = T_{Low}$ to T_{High}			–	0.4	2.0	
Average Temperature Coefficient of Input Offset Current	6	$\lvert TC_{Iio}\rvert$				nA/°C
$T_A = T_{Low}$ to T_{High}			–	2.5	–	
Output Offset Current T_A = + 25°C	6	$\lvert I_{OO}\rvert$		10	50	µA
$\lvert I_{14} - I_2\rvert$ $T_A = T_{Low}$ to T_{High}			–	20	100	
Average Temperature Coefficient of Output Offset Current	6	$\lvert TC_{IOO}\rvert$				nA/°C
$T_A = T_{Low}$ to T_{High}			–	20	–	
Frequency Response	9,10					
3.0 dB Bandwidth, R_L = 11 kΩ		$BW_{(3dB)}$	–	3.0	–	MHz
3.0 dB Bandwidth, R_L = 50 Ω (Transconductance Bandwidth)		$T_{BW(3dB)}$	–	80	–	MHz
3° Relative Phase Shift Between V_X and V_Y		fϕ	–	750	–	kHz
1% Absolute Error Due to Input-Output Phase Shift		fθ	–	30	–	kHz
Common Mode Input Swing	11	CMV				Vdc
(Either Input)			±10.5	±12	–	
Common Mode Gain T_A = + 25°C	11	A_{CM}	– 50	– 60	–	dB
(Either Input) $T_A = T_{Low}$ to T_{High}			– 40	– 50	–	
Common Mode Quiescent	12	V_{O1}	–	21	–	Vdc
Output Voltage		V_{O2}	–	21	–	
Differential Output Voltage Swing Capability	9	V_O	–	±14	–	V_{pk}
Power Supply Sensitivity	12	S^+	–	5.0	–	mV/V
		S^-	–	10	–	
Power Supply Current	12	I_7	–	6.0	7.0	mA
DC Power Dissipation	12	P_D	–	135	170	mW

NOTES: 1. T_{High} = +70°C for MC1495 = +125°C for MC1495B T_{Low} = 0°C for MC1495 = – 40°C for MC1495B

Figure 1. Multiplier Transfer Characteristic

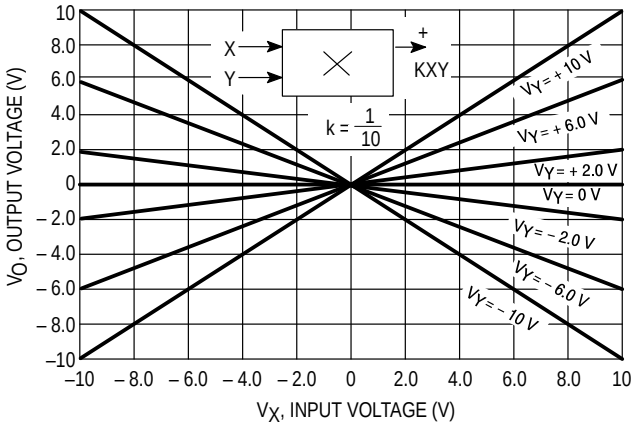


Figure 2. Transconductance Bandwidth

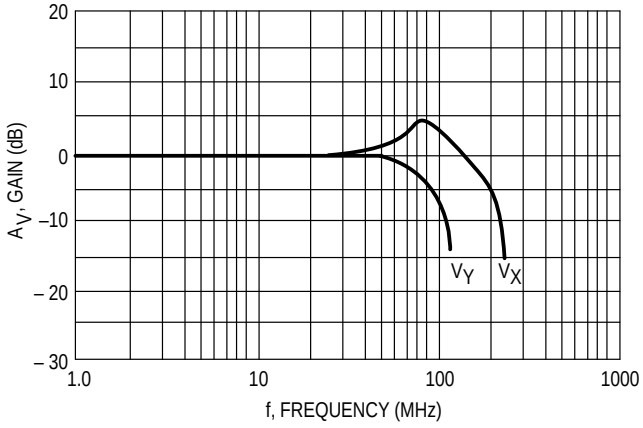
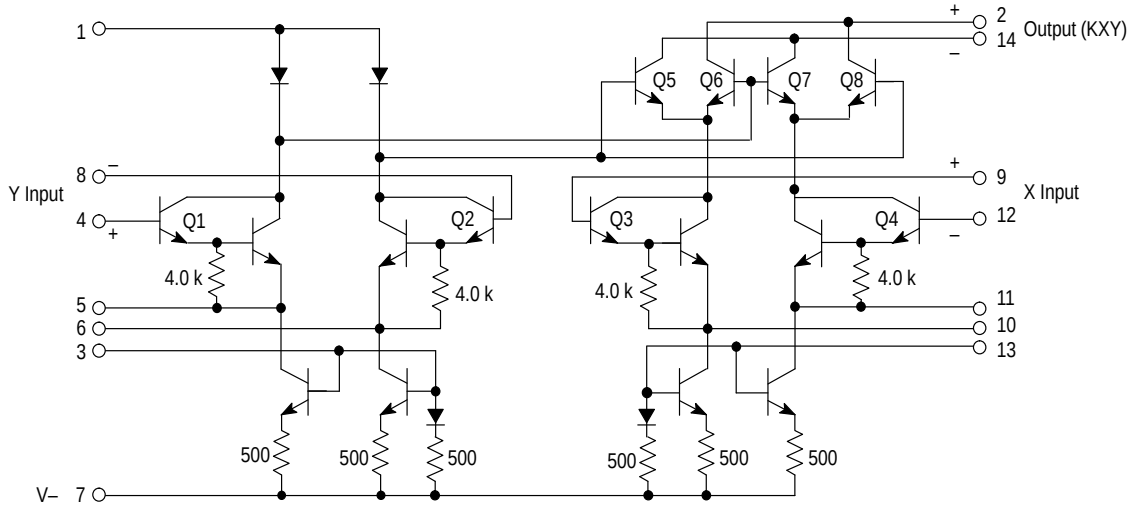
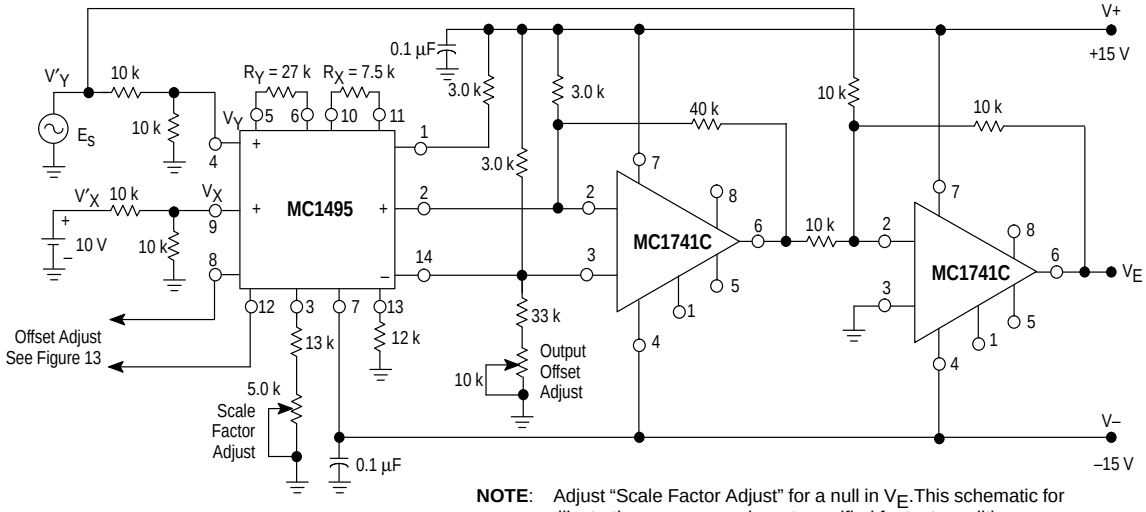


Figure 3. Circuit Schematic



This device contains 16 active transistors.

Figure 4. Linearity (Using Null Technique)



NOTE: Adjust “Scale Factor Adjust” for a null in V_E.This schematic for illustrative purposes only, not specified for test conditions.

Figure 5. Linearity (Using X-Y Plotter Technique)

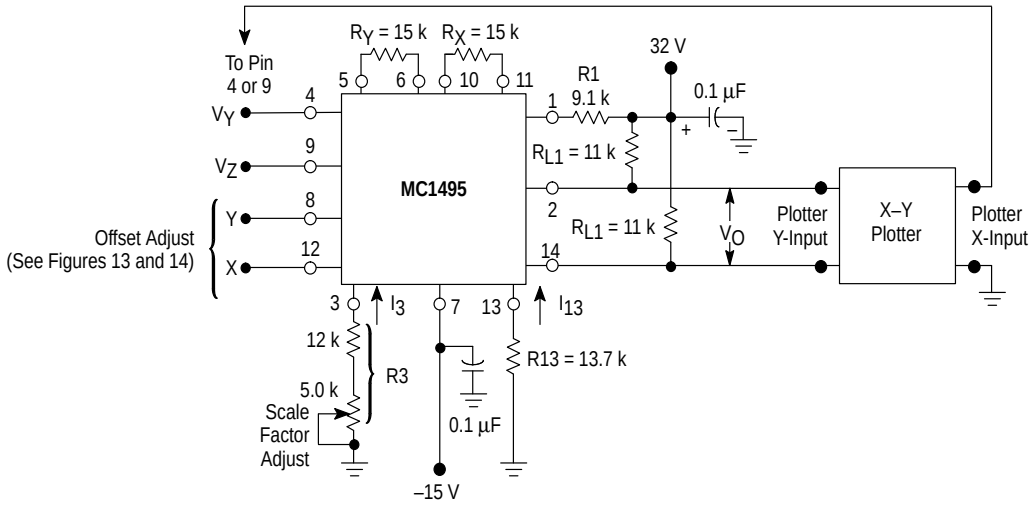


Figure 6. Input and Output Current

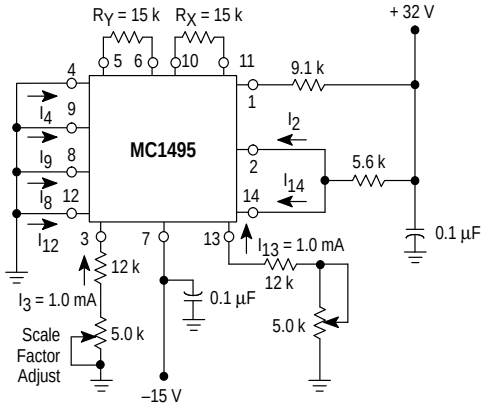


Figure 7. Input Resistance

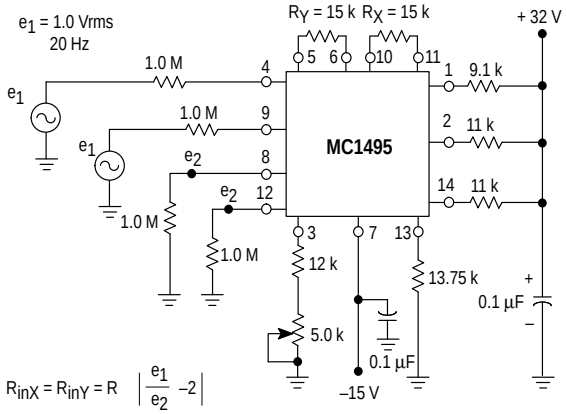


Figure 8. Output Resistance

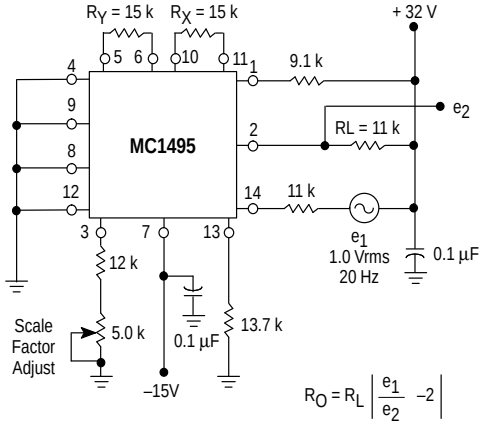


Figure 9. Bandwidth (R_L = 11 kΩ)

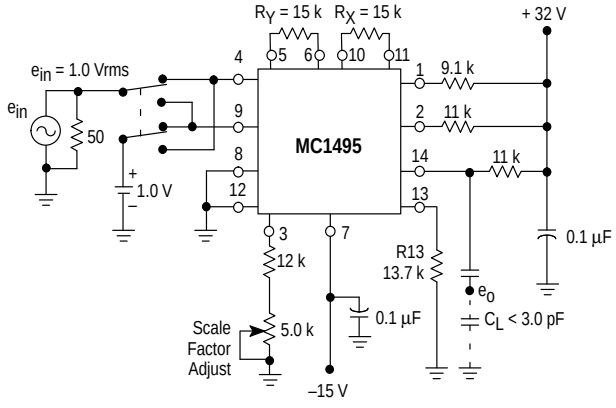


Figure 10. Bandwidth (R_L = 50 Ω)

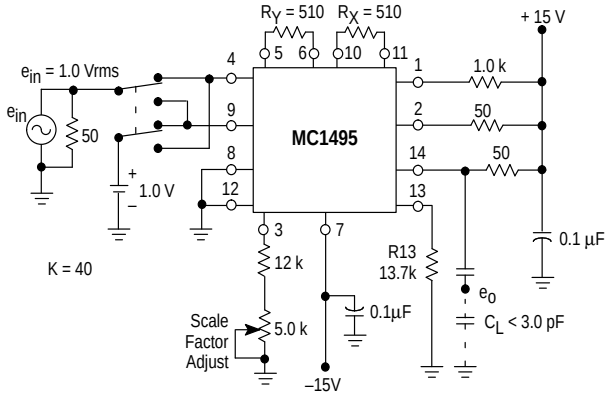


Figure 11. Common Mode Gain and Common Mode Input Swing

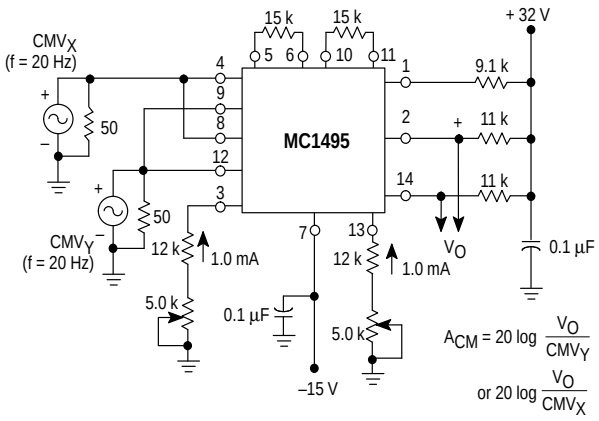


Figure 12. Power Supply Sensitivity

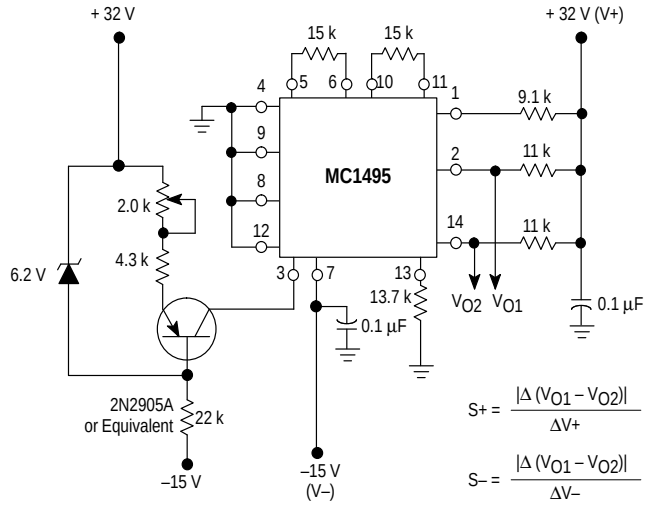
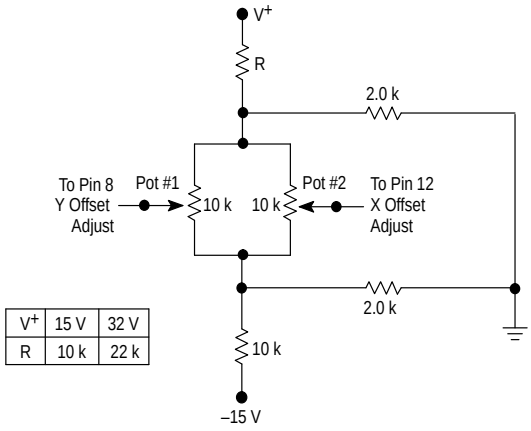
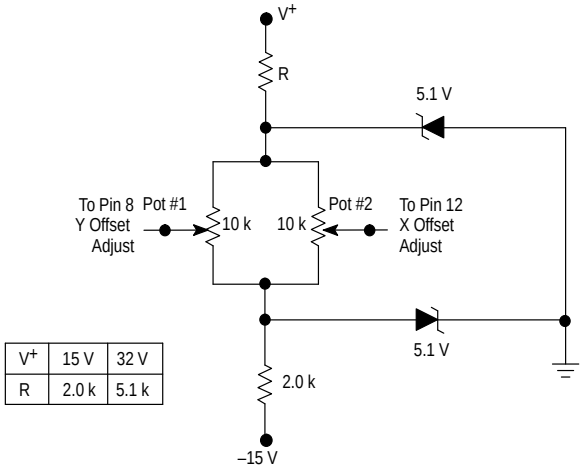


Figure 13. Offset Adjust Circuit



V+	15 V	32 V
R	10 k	22 k

Figure 14. Offset Adjust Circuit (Alternate)



V+	15 V	32 V
R	2.0 k	5.1 k

Figure 15. Linearity versus Temperature

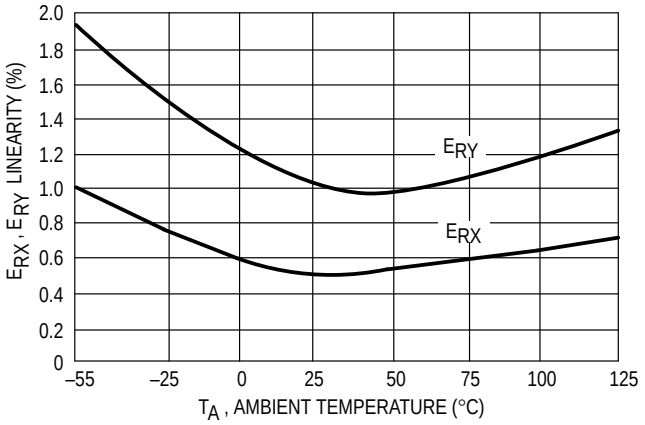


Figure 16. Scale Factor versus Temperature

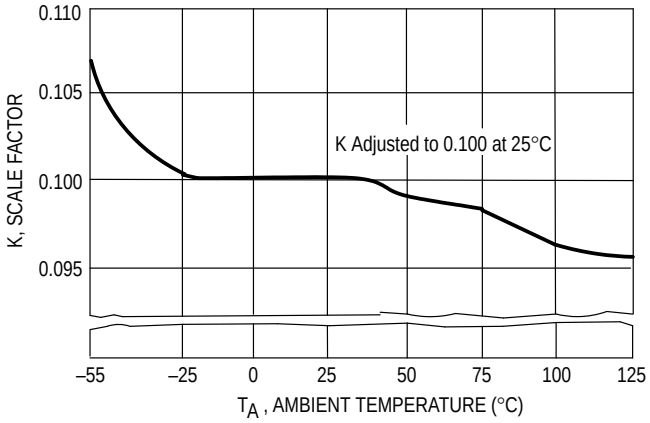


Figure 17. Error Contributed by Input Differential Amplifier

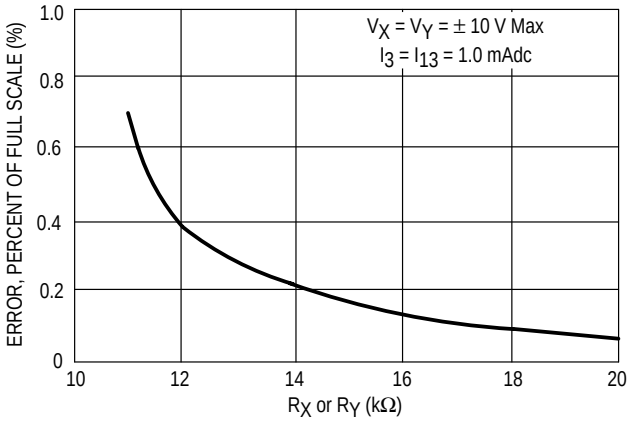


Figure 18. Error Contributed by Input Differential Amplifier

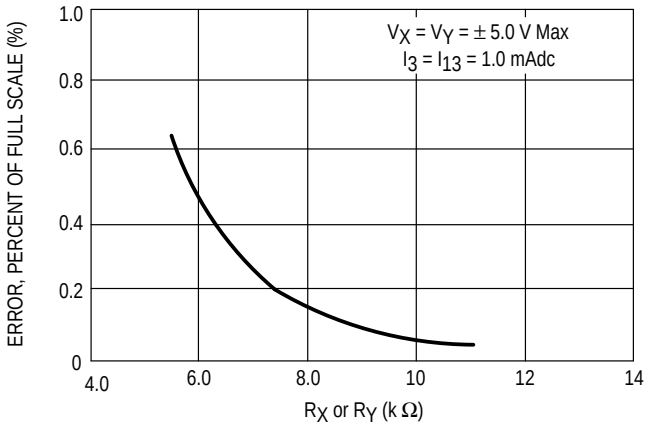
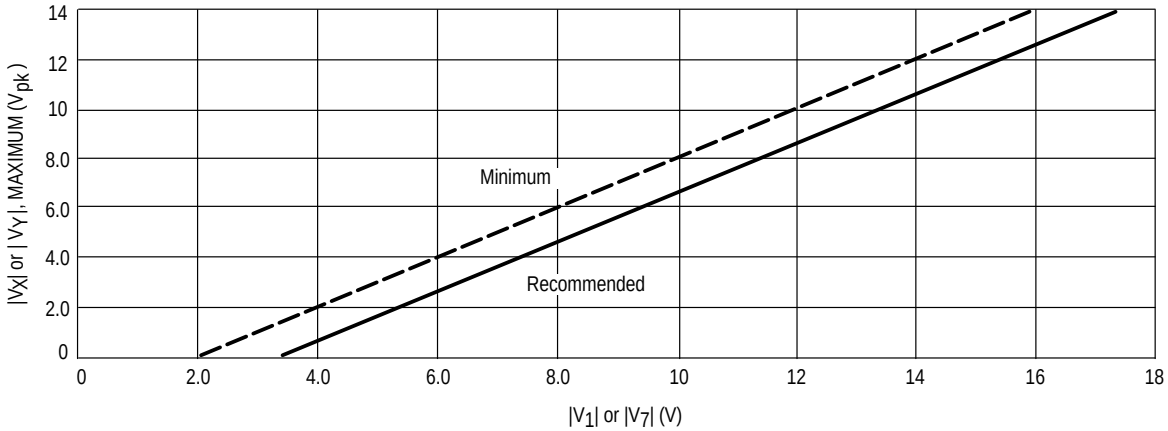


Figure 19. Maximum Allowable Input Voltage versus Voltage at Pin 1 or Pin 7



OPERATION AND APPLICATIONS INFORMATION

Theory of Operation

The MC1495 is a monolithic, four-quadrant multiplier which operates on the principle of variable transconductance. A detailed theory of operation is covered in Application Note AN489, *Analysis and Basic Operation of the MC1595*. The result of this analysis is that the differential output current of the multiplier is given by:

$$I_A - I_B = \Delta I = \frac{2V_X V_Y}{R_X R_Y I_3}$$

where, I_A and I_B are the currents into Pins 14 and 2, respectively, and V_X and V_Y are the X and Y input voltages at the multiplier input terminals.

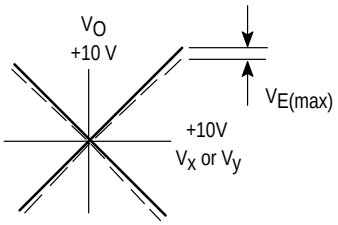
DESIGN CONSIDERATIONS

General

The MC1495 permits the designer to tailor the multiplier to a specific application by proper selection of external components. External components may be selected to optimize a given parameter (e.g. bandwidth) which may in turn restrict another parameter (e.g. maximum output voltage swing). Each important parameter is discussed in detail in the following paragraphs.

Linearity, Output Error, E_{RX} or E_{RY}

Linearity error is defined as the maximum deviation of output voltage from a straight line transfer function. It is expressed as error in percent of full scale (see figure below).



For example, if the maximum deviation, $V_{E(max)}$, is ±100 mV and the full scale output is 10 V, then the percentage error is:

$$E_R = \frac{V_{E(max)}}{V_{O(max)}} \times 100 = \frac{100 \times 10^{-3}}{10} \times 100 = \pm 1.0\%.$$

Linearity error may be measured by either of the following methods:

1. Using an X-Y plotter with the circuit shown in Figure 5, obtain plots for X and Y similar to the one shown above.
2. Use the circuit of Figure 4. This method nulls the level shifted output of the multiplier with the original input.The peak output of the null operational amplifier will be equal to the error voltage, $V_{E\ (max)}$.

One source of linearity error can arise from large signal nonlinearity in the X and Y input differential amplifiers. To avoid introducing error from this source, the emitter degeneration resistors R_X and R_Y must be chosen large enough so that nonlinear base-emitter voltage variation can be ignored. Figures 17 and 18 show the error expected from this source as a function of the values of R_X and R_Y with an operating current of 1.0 mA in each side of the differential amplifiers (i.e., $I_3 = I_{13} = 1.0$ mA).

3 dB Bandwidth and Phase Shift

Bandwidth is primarily determined by the load resistors and the stray multiplier output capacitance and/or the operational amplifier used to level shift the output. If wideband operation is desired, low value load resistors and/or a wideband operational amplifier should be used. Stray output capacitance will depend to a large extent on circuit layout.

Phase shift in the multiplier circuit results from two sources: phase shift common to both X and Y channels (due to the load resistor-output capacitance pole mentioned above) and relative phase shift between X and Y channels (due to differences in transadmittance in the X and Y channels). If the input to output phase shift is only 0.6°, the output product of two sine waves will exhibit a vector error of 1%. A 3° relative phase shift between V_X and V_Y results in a vector error of 5%.

Maximum Input Voltage

$V_{X(max)}$, $V_{Y(max)}$ input voltages must be such that:

$$V_{X(max)} < I_{13} R_Y$$
$$V_{Y(max)} < I_3 R_Y$$

Exceeding this value will drive one side of the input amplifier to “cutoff” and cause nonlinear operation.

Current I_3 and I_{13} are chosen at a convenient value (observing power dissipation limitation) between 0.5 mA and 2.0 mA, approximately 1.0 mA. Then R_X and R_Y can be determined by considering the input signal handling requirements.

For $V_{X(max)} = V_{Y(max)} = 10$ V;

$$R_X = R_Y > \frac{10\ V}{1.0\ mA} = 10\ k\Omega.$$

The equation $I_A - I_B = \dfrac{2V_X\ V_Y}{R_X\ R_Y\ I_3}$

is derived from $I_A - I_B = \dfrac{2V_X\ V_Y}{(R_X + \frac{2kT}{qI_{13}})\ (R_Y + \frac{2kT}{qI_3})\ I_3}$

with the assumption $R_X >> \dfrac{2kT}{qI_{13}}$ and $R_Y >> \dfrac{2kT}{qI_3}$.

At $T_A = +25°C$ and $I_{13} = I_3 = 1.0$ mA,

$$\frac{2kT}{qI_{13}} = \frac{2kT}{qI_3} = 52\ \Omega.$$

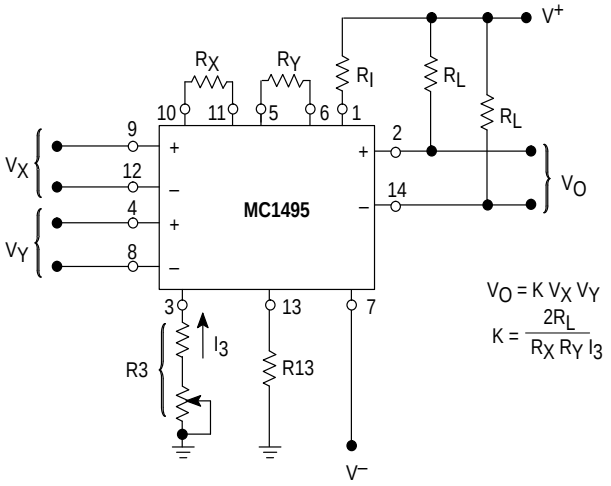
Therefore, with $R_X = R_Y = 10$ kΩ the above assumption is valid. Reference to Figure 19 will indicate limitations of $V_{X(max)}$ or $V_{Y(max)}$ due to V_1 and V_7. Exceeding these limits will cause saturation or “cutoff” of the input transistors. See Step 4 of General Design Procedure for further details.

Maximum Output Voltage Swing

The maximum output voltage swing is dependent upon the factors mentioned below and upon the particular circuit being considered.

For Figure 20 the maximum output swing is dependent upon V^+ for positive swing and upon the voltage at Pin 1 for negative swing. The potential at Pin 1 determines the quiescent level for transistors Q_5, Q_6, Q_7 and Q_8. This potential should be related so that negative swing at Pins 2 or 14 does not saturate those transistors. See General Design Procedure for further information regarding selection of these potentials.

Figure 20. Basic Multiplier



If an operational amplifier is used for level shift, as shown in Figure 21, the output swing (of the multiplier) is greatly reduced. See Section 3 for further details.

GENERAL DESIGN PROCEDURE

Selection of component values is best demonstrated by the following example. Assume resistive dividers are used at the X and Y-inputs to limit the maximum multiplier input to ± 5.0 V [$V_X = V_{Y(max)}$] for a ± 10 V input [$V_{X'} = V_{Y'(max)}$] (see Figure 21). If an overall scale factor of 1/10 is desired,

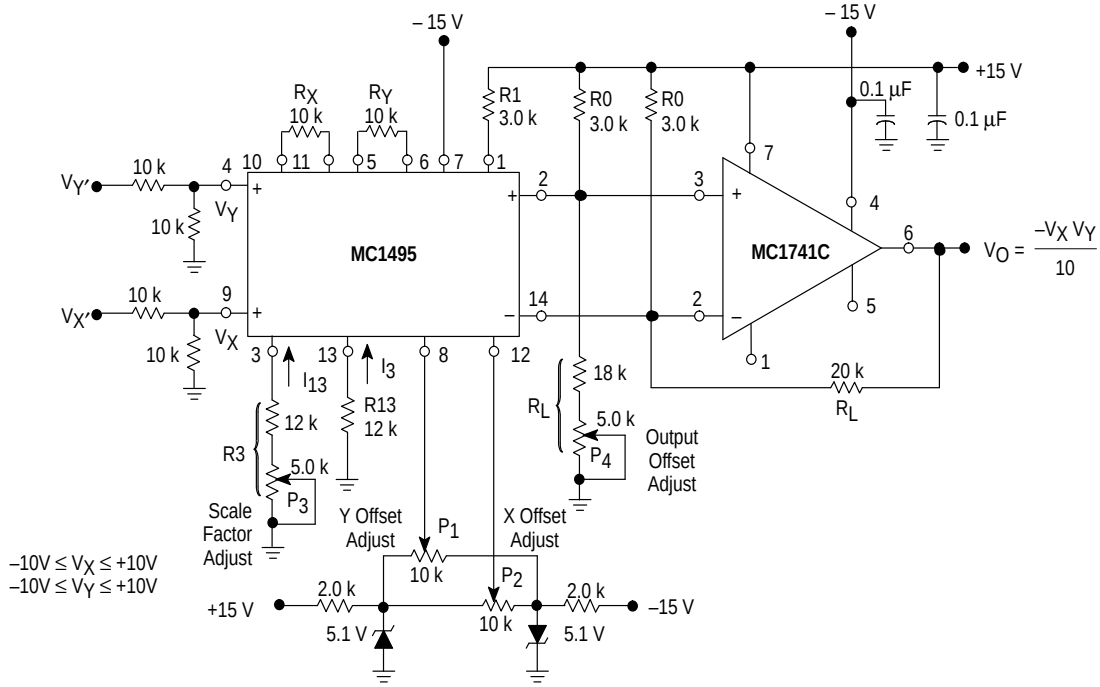
$$\text{then, } V_O = \frac{V_{X'}\, V_{Y'}}{10} = \frac{(2V_X)\,(2V_Y)}{10} = 4/10\ V_X\, V_Y$$

Therefore, K = 4/10 for the multiplier (excluding the divider network).

Step 1. The fist step is to select current I_3 and current I_{13}. There are no restrictions on the selection of either of these currents except the power dissipation of the device. I_3 and I_{13} will normally be 1.0 mA or 2.0 mA. Further, I_3 does not have to be equal to I_{13}, and there is normally no need to make them different. For this example, let

$$I_3 = I_{13} = 1.0\ \text{mA}.$$

Figure 21. Multiplier with Operational Amplifier Level Shift



To set currents I_3 and I_{13} to the desired value, it is only necessary to connect a resistor between Pin 13 and ground, and between Pin 3 and ground. From the schematic shown in Figure 3, it can be seen that the resistor values necessary are given by:

$$R13 + 500\ \Omega = \frac{|V-| - 0.7\ V}{I_{13}}$$

$$R3 + 500\ \Omega = \frac{|V-| - 0.7\ V}{I_3}$$

Let V– = –15 V, then $R13 + 500 = \frac{14.3\ V}{1.0\ mA}$ or R13 = 13.8 kΩ

Let R_{13} = 12 kΩ. Similarly, R_3 = 13.8 kΩ, let R_3 = 15 kΩ

However, for applications which require an accurate scale factor, the adjustment of R_3 and consequently, I_3, offers a convenient method of making a final trim of the scale factor. For this reason, as shown in Figure 21, resistor R_3 is shown as a fixed resistor in series with a potentiometer.

For applications not requiring an exact scale factor (balanced modulator, frequency doubler, AGC amplifier, etc.) Pins 3 and 13 can be connected together and a single resistor from Pin 3 to ground can be used. In this case, the single resistor would have a value of 1/2 the above calculated value for R_{13}.

Step 2. The next step is to select R_X and R_Y. To insure that the input transistors will always be active, the following conditions should be met:

$$\frac{V_X}{R_X} < I_{13}, \qquad \frac{V_Y}{R_Y} < I_3$$

A good rule of thumb is to make $I_3R_Y \geq 1.5\ V_{Y(max)}$ and $I_{13}R_X \geq 1.5\ V_{X(max)}$. The larger the I_3R_Y and $I_{13}R_X$ product in relation to V_Y and V_X respectively, the more accurate the multiplier will be (see Figures 17 and 18).

Let $R_X = R_Y$ = 10 kΩ,
then I_3R_Y = 10 V
$I_{13}R_X$ = 10 V

since $V_{X(max)} = V_{Y(max)} = 5.0$ V, the value of $R_X = R_Y$ = 10 kΩ is sufficient.

Step 3. Now that R_X, R_Y and I_3 have been chosen, R_L can be determined:

$$K = \frac{2R_L}{R_X\ R_Y\ I_3} = \frac{4}{10}\ , \text{ or } \frac{(2)\ (R_L)}{(10\ k)\ (10\ k)\ (1.0\ mA)} = \frac{4}{10}$$

Thus R_L = 20 kΩ.

Step 4. To determine what power supply voltage is necessary for this application, attention must be given to the circuit schematic shown in Figure 3. From the circuit schematic it can be seen that in order to maintain transistors Q_1, Q_2, Q_3 and Q_4 in an active region when the maximum input voltages are applied ($V_{X'} = V_{Y'}$ = 10 V or V_X = 5.0 V, V_Y = 5.0 V), their respective collector voltage should be at least a few tenths of a volt higher than the maximum input voltage. It should also be noticed that the collector voltage of transistors Q_3 and Q_4 is at a potential which is two diode-drops below the voltage at Pin 1. Thus, the voltage at Pin 1 should be about 2.0 V higher than the maximum input voltage. Therefore, to handle +5.0 V at the inputs, the voltage at Pin 1 must be at least +7.0 V. Let V_1 = 9.0 Vdc.

Since the current flowing into Pin 1 is always equal to $2I_3$, the voltage at Pin 1 can be set by placing a resistor (R_1) from Pin 1 to the positive supply:

$$R_1 = \frac{V^+ - V_1}{2I_3}$$

Let V+ = 15 V, then $R_1 = \frac{15\ V - 9.0\ V}{(2)\ (1.0\ mA)}$

$$R_1 = 3.0\ \ k\Omega.$$

Note that the voltage at the base of transistors Q_5, Q_6, Q_7 and Q_8 is one diode-drop below the voltage at Pin 1. Thus, in order that these transistors stay active, the voltage at Pins 2 and 14 should be approximately halfway between the voltage at Pin 1 and the positive supply voltage. For this example, the voltage at Pins 2 and 14 should be approximately 11 V.

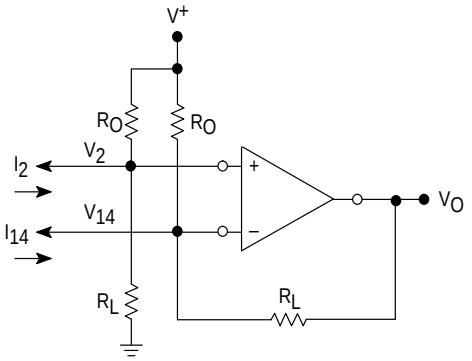
Step 5. For dc applications, such as the multiply, divide and square-root functions, it is usually desirable to convert the differential output to a single-ended output voltage referenced to ground. The circuit shown in Figure 22 performs this function. It can be shown that the output voltage of this circuit is given by:

$$V_O = (I_2 - I_{14})\ R_L$$

And since $I_A - I_B = I_2 - I_{14} = \frac{2I_X\ I_Y}{I_3} = \frac{2V_XV_Y}{I_3R_XR_Y}$

then $V_O = \frac{2R_L\ V_{X'}\ V_{Y'}}{4R_X\ R_X\ I_3}$ where, $V_{X'}$ $V_{Y'}$ is the voltage at the input to the voltage dividers.

Figure 22. Level Shift Circuit



The choice of an operational amplifier for this application should have low bias currents, low offset current, and a high common mode input voltage range as well as a high common mode rejection ratio. The MC1456, and MC1741C operational amplifiers meet these requirements.

Referring to Figure 21, the level shift components will be determined. When $V_X = V_Y = 0$, the currents I_2 and I_{14} will be equal to I_{13}. In Step 3, R_L was found to be 20 kΩ and in Step 4, V_2 and V_{14} were found to be approximately 11 V. From this information R_O can be found easily from the following equation (neglecting the operational amplifiers bias current):

$$\frac{V2}{R_L} + I_{13} = \frac{V^+ - V_2}{R_O}$$

And for this example, $\frac{11\ V}{20\ k\Omega} + 1.0\ mA = \frac{15\ V - 11\ V}{R_O}$

Solving for R_O: $R_O = 2.6\ k\Omega$, thus, select $R_O = 3.0\ k\Omega$

For $R_O = 3.0\ k\Omega$, the voltage at Pins 2 and 14 is calculated to be:

$$V_2 = V_{14} = 10.4\ V.$$

The linearity of this circuit (Figure 21) is likely to be as good or better than the circuit of Figure 5. Further improvements are possible as shown in Figure 23 where R_Y has been increased substantially to improve the Y linearity, and R_X decreased somewhat so as not to materially affect the X linearity. This avoids increasing R_L significantly in order to maintain a K of 0.1.

The versatility of the MC1495 allows the user to to optimize its performance for various input and output signal levels.

OFFSET AND SCALE FACTOR ADJUSTMENT

Offset Voltages

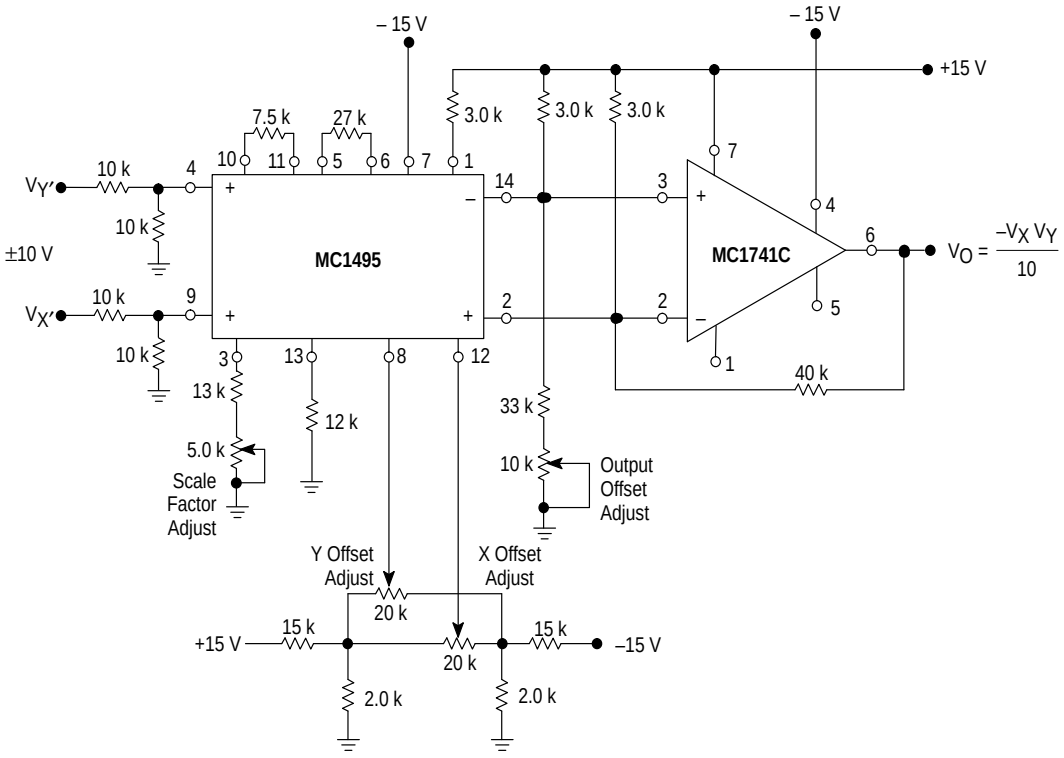
Within the monolithic multiplier (Figure 3) transistor base-emitter junctions are typically matched within 1.0 mV and resistors are typically matched within 2%. Even with this careful matching, an output error can occur. This output error is comprised of X-input offset voltage, Y-input offset voltage, and output offset voltage. These errors can be adjusted to zero with the techniques shown in Figure 21. Offset terms can be shown analytically by the transfer function:

$$V_O = K[V_X \pm V_{iox} \pm V_{x(off)}]\,[V_y \pm V_{ioy} \pm V_{y(off)}] \pm V_{OO} \quad (1)$$

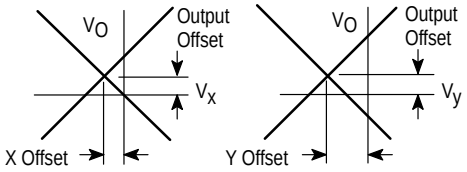
Where:

K = scale factor
V_X = "x" input voltage
V_y = "y" input voltage
V_{iox} = "x" input offset voltage
V_{ioy} = "y" input offset voltage
$V_{X(off)}$ = "x" input offset adjust voltage
$V_{y(off)}$ = "y" input offset adjust voltage
V_{OO} = output offset voltage.

Figure 23. Multiplier with Improved Linearity



X, Y and Output Offset Voltages



For most dc applications, all three offset adjust potentiometers (P_1, P_2, P_4) will be necessary. One or more offset adjust potentiometers can be eliminated for ac applications (see Figures 28, 29, 30, 31).

If well regulated supply voltages are available, the offset adjust circuit of Figure 13 is recommended. Otherwise, the circuit of Figure 14 will greatly reduce the sensitivity to power supply changes.

Scale Factor

The scale factor K is set by P_3 (Figure 21). P_3 varies I_3 which inversely controls the scale factor K. It should be noted that current I_3 is one-half the current through R_1. R_1 sets the bias level for Q_5, Q_6, Q_7, and Q_8 (see Figure 3). Therefore, to be sure that these devices remain active under all conditions of input and output swing, care should be exercised in adjusting P_3 over wide voltage ranges (see General Design Procedure).

Adjustment Procedures

The following adjustment procedure should be used to null the offsets and set the scale factor for the multiply mode of operation, (see Figure 21).

1. X-Input Offset
   (a) Connect oscillator (1.0 kHz, 5.0 V_{pp} sinewave) to the Y-input (Pin 4).
   (b) Connect X-input (Pin 9) to ground.
   (c) Adjust X offset potentiometer (P_2) for an ac null at the output.
2. Y-Input Offset
   (a) Connect oscillator (1.0 kHz, 5.0 V_{pp} sinewave) to the X-input (Pin 9).
   (b) Connect Y-input (Pin 4) to ground.
   (c) Adjust Y offset potentiometer (P_1) for an ac null at the output.
3. Output Offset
   (a) Connect both X and Y-inputs to ground.
   (b) Adjust output offset potentiometer (P_4) until the output voltage (V_O) is 0 Vdc.
4. Scale Factor
   (a) Apply +10 Vdc to both the X and Y-inputs.
   (b) Adjust P_3 to achieve + 10 V at the output.
5. Repeat steps 1 through 4 as necessary.

The ability to accurately adjust the MC1495 depends upon the characteristics of potentiometers P_1 through P_4. Multi-turn, infinite resolution potentiometers with low temperature coefficients are recommended.

DC APPLICATIONS

Multiply

The circuit shown in Figure 21 may be used to multiply signals from dc to 100 kHz. Input levels to the actual multiplier are 5.0 V (max). With resistive voltage dividers the maximum could be very large however, for this application two-to-one dividers have been used so that the maximum input level is 10 V. The maximum output level has also been designed for 10 V (max).

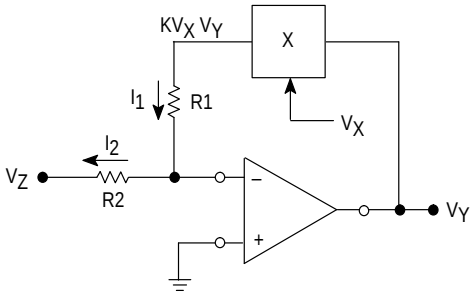
Squaring Circuit

If the two inputs are tied together, the resultant function is squaring; that is $V_O = KV^2$ where K is the scale factor. Note that all error terms can be eliminated with only three adjustment potentiometers, thus eliminating one of the input offset adjustments. Procedures for nulling with adjustments are given as follows:

A. AC Procedure:
   1. Connect oscillator (1.0 kHz, 15 V_{pp}) to input.
   2. Monitor output at 2.0 kHz with tuned voltmeter and adjust P_3 for desired gain. (Be sure to peak response of the voltmeter.)
   3. Tune voltmeter to 1.0 kHz and adjust P_1 for a minimum output voltage.
   4. Ground input and adjust P_4 (output offset) for 0 Vdc output.
   5. Repeat steps 1 through 4 as necessary.

B. DC Procedure:
   1. Set $V_X = V_Y = 0$ V and adjust P_4 (output offset potentiometer) such that $V_O = 0$ Vdc
   2. Set $V_X = V_Y = 1.0$ V and adjust P_1 (Y-input offset potentiometer) such that the output voltage is + 0.100 V.
   3. Set $V_X = V_Y = 10$ Vdc and adjust P_3 such that the output voltage is + 10 V.
   4. Set $V_X = V_Y = –10$ Vdc. Repeat steps 1 through 3 as necessary.

Figure 24. Basic Divide Circuit



Divide Circuit

Consider the circuit shown in Figure 24 in which the multiplier is placed in the feedback path of an operational amplifier. For this configuration, the operational amplifier will maintain a “virtual ground” at the inverting (–) input. Assuming that the bias current of the operational amplifier is negligible, then $I_1 = I_2$ and,

$$\frac{KV_XV_Y}{R1} = \frac{-V_Z}{R2} \quad (1)$$

$$\text{Solving for } V_Y, \quad V_Y = \frac{-R1}{R2\ K}\frac{V_Z}{V_X} \quad (2)$$

$$\text{If R1=R2,} \quad V_Y = \frac{-V_Z}{KV_X} \quad (3)$$

$$\text{If R1= KR2,} \quad V_Y = \frac{-V_Z}{V_X} \quad (4)$$

Hence, the output voltage is the ratio of V_Z to V_X and provides a divide function. This analysis is, of course, the ideal condition. If the multiplier error is taken into account, the output voltage is found to be:

$$V_Y = -\left[\frac{R1}{R2\ K}\right]\frac{V_Z}{V_X} + \frac{\Delta E}{KV_X} \quad (5)$$

where ΔE is the error voltage at the output of the multiplier. From this equation, it is seen that divide accuracy is strongly dependent upon the accuracy at which the multiplier can be set, particularly at small values of V_Y. For example, assume that R1 = R2, and K = 1/10. For these conditions the output of the divide circuit is given by:

$$V_Y = \frac{-10\ V_Z}{V_X} + \frac{10\ \Delta E}{V_X} \quad (6)$$

From Equation 6, it is seen that only when V_X = 10 V is the error voltage of the divide circuit as low as the error of the multiply circuit. For example, when V_X is small, (0.1 V) the error voltage of the divide circuit can be expected to be a hundred times the error of the basic multiplier circuit.

In terms of percentage error,

$$\text{percentage error} = \frac{\text{error}}{\text{actual}} \times 100\%$$

or from Equation (5),

$$PE_D = \frac{\frac{\Delta E}{KV_X}}{\left[\frac{R1}{R2\ K}\right]\frac{V_Z}{V_X}} = \left[\frac{R2}{R1}\right]\frac{\Delta E}{V_Z} \quad (7)$$

From Equation 7, the percentage error is inversely related to voltage V_Z (i.e., for increasing values of V_Z, the percentage error decreases).

A circuit that performs the divide function is shown in Figure 25.

Two things should be emphasized concerning Figure 25.

1. The input voltage ($V_{X'}$) must be greater than zero and must be positive. This insures that the current out of Pin 2 of the multiplier will always be in a direction compatible with the polarity of V_Z.
2. Pin 2 and 14 of the multiplier have been interchanged in respect to the operational amplifiers input terminals. In this instance, Figure 25 differs from the circuit connection shown in Figure 21; necessitated to insure negative feedback around the loop.

A suggested adjustment procedure for the divide circuit.

1. Set V_Z = 0 V and adjust the output offset potentiometer (P_4) until the output voltage (V_O) remains at some (not necessarily zero) constant value as $V_{X'}$ is varied between +1.0 V and +10 V.
2. Keep V_Z at 0 V, set $V_{X'}$ at +10 V and adjust the Y input offset potentiometer (P_1) until V_O = 0 V.
3. Let $V_{X'} = V_Z$ and adjust the X-input offset potentiometer ($P_{2)}$ until the output voltage remains at some (not necessarily – 10 V) constant value as $V_Z = V_{X'}$ is varied between +1.0 and +10 V.
4. Keep $V_{X'} = V_Z$ and adjust the scale factor potentiometer (P_3) until the average value of V_O is –10 V as $V_Z = V_{X'}$ is varied between +1.0 V and +10 V.
5. Repeat steps 1 through 4 as necessary to achieve optimum performance.

Figure 25. Divide Circuit

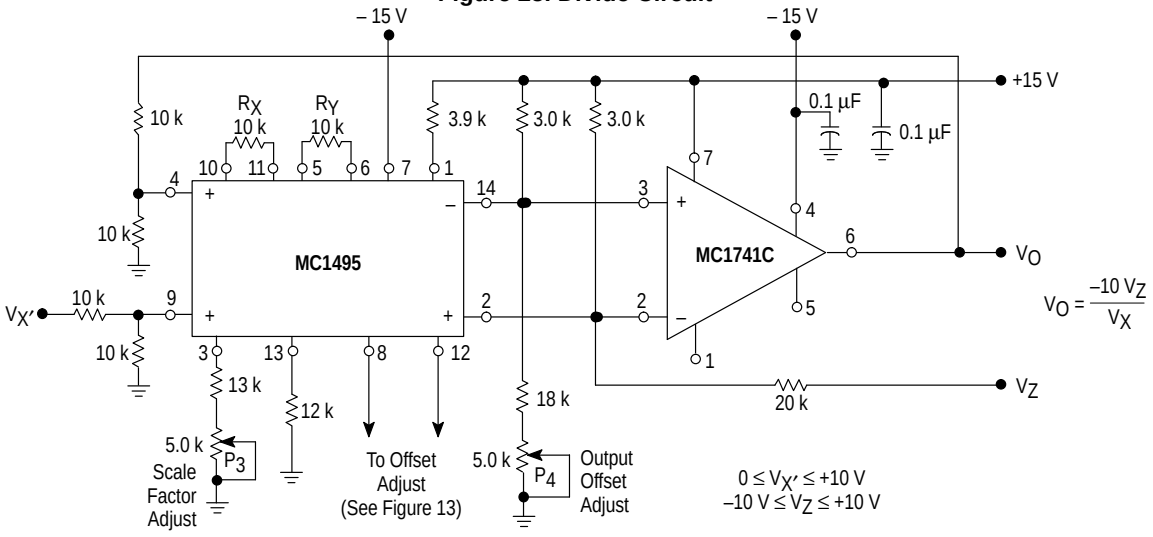
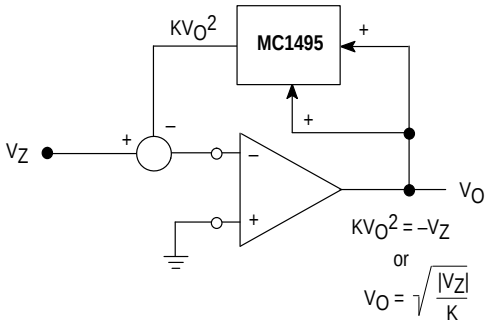


Figure 26. Basic Square Root Circuit



Square Root

A special case of the divide circuit in which the two inputs to the multiplier are connected together is the square root function as indicated in Figure 26. This circuit may suffer from latch-up problems similar to those of the divide circuit. Note that only one polarity of input is allowed and diode clamping (see Figure 27) protects against accidental latch-up.

This circuit also may be adjusted in the closed-loop mode as follows:

1. Set V_Z to –0.01 V and adjust P_4 (output offset) for V_O = +0.316 V, being careful to approach the output from the positive side to preclude the effect of the output diode clamping.
2. Set V_Z to –0.9 V and adjust P_2 (X adjust) for V_O = +3.0 V.
3. Set V_Z to –10 V and adjust P_3 (scale factor adjust) for V_O = +10 V.
4. Steps 1 through 3 may be repeated as necessary to achieve desired accuracy.

AC APPLICATIONS

The applications that follow demonstrate the versatility of the monolithic multiplier. If a potted multiplier is used for these cases, the results generally would not be as good because the potted units have circuits that, although they optimize dc multiplication operation, can hinder ac applications.

Frequency doubling often is done with a diode where the fundamental plus a series of harmonics are generated. However, extensive filtering is required to obtain the desired harmonic, and the second harmonic obtained under this technique usually is small in magnitude and requires amplification.

When a multiplier is used to double frequency the second harmonic is obtained directly, except for a dc term, which can be removed with ac coupling.

$$e_o = KE^2 \cos^2 \omega t$$

$$e_o = \frac{KE^2}{2} (1 + \cos 2\omega t).$$

A potted multiplier can be used to obtain the double frequency component, but frequency would be limited by its internal level-shift amplififer. In the monolithic units, the amplifier is omitted.

In a typical doubler circuit, conventional ± 15 V supplies are used. An input dynamic range of 5.0 V peak-to-peak is allowed. The circuit generates wave-forms that are double frequency; less than 1% distortion is encountered without filtering. The configuration has been successfully used in excess of 200 kHz; reducing the scale factor by decreasing the load resistors can further expand the bandwidth.

Figure 29 represents an application for the monolithic multiplier as a balanced modulator. Here, the audio input signal is 1.6 kHz and the carrier is 40 kHz.

Figure 27. Square Root Circuit

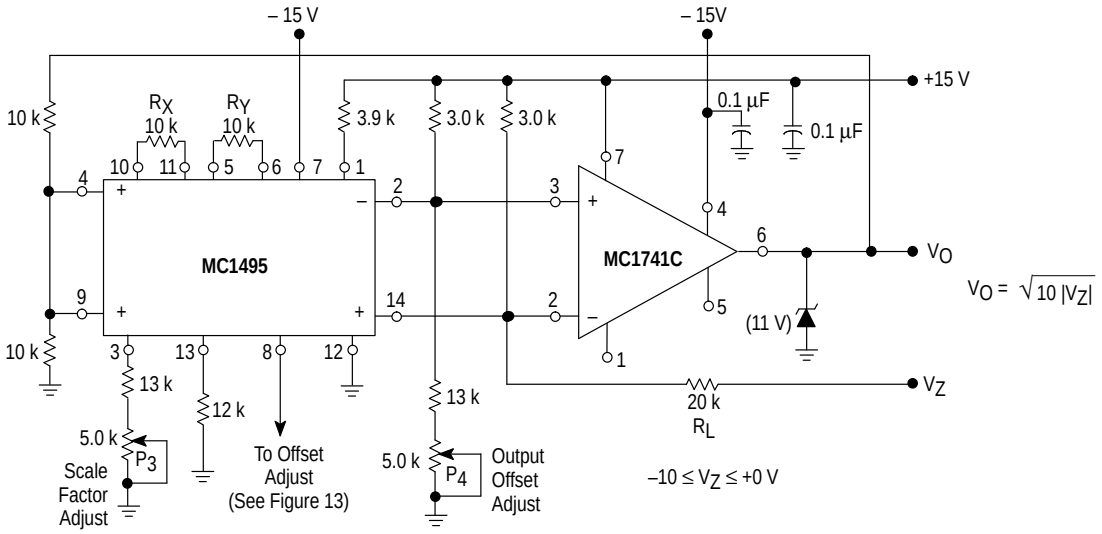
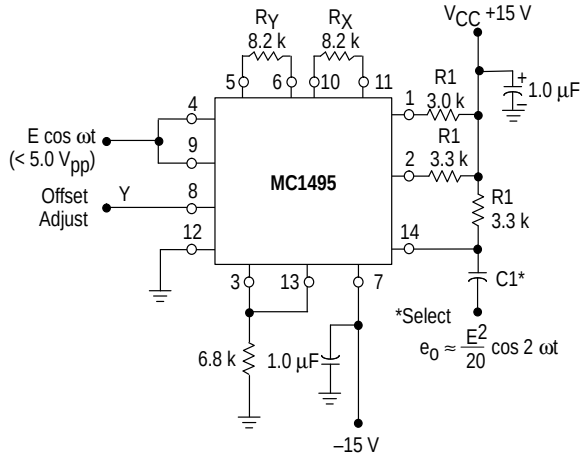


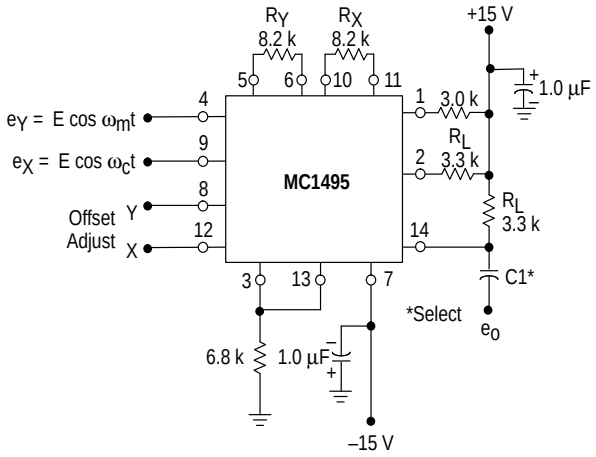
Figure 28. Frequency Doubler



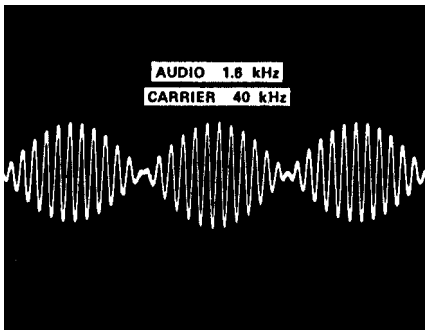
When two equal cosine waves are applied to X and Y, the result is a wave shape of twice the input frequency. For this example the input was a 10 kHz signal, output was 20 kHz.

Figure 29. Balanced Modulator

(A)



(B)



The defining equation for balanced modulation is

$$K(E_m \cos \omega_m t)(E_c \cos \omega_c t) =$$

$$\frac{KE_c E_m}{2} [\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m)t]$$

where ω_c is the carrier frequency, ω_m is the modulator frequency and K is the multiplier gain constant.

AC coupling at the output eliminates the need for level translation or an operational amplifier; a higher operating frequency results.

A problem common to communications is to extract the intelligence from single-sideband received signal. The ssb signal is of the form:

$$e_{ssb} = A \cos(\omega_c + \omega_m) t$$

and if multiplied by the appropriate carrier waveform, cos $\omega_c t$,

$$e_{ssb} e_{carrier} = \frac{AK}{2} [\cos(2\omega_c + \omega_m)t + \cos(\omega_c) t].$$

If the frequency of the band-limited carrier signal (ω_c) is ascertained in advance, the designer can insert a low pass filter and obtain the (AK/2) (cos$\omega_c t$) term with ease. He/she also can use an operational amplifier for a combination level shift-active filter, as an external component. But in potted multipliers, even if the frequency range can be covered, the operational amplifier is inside and not accessible, so the user must accept the level shifting provided, and still add a low pass filter.

Amplitude Modulation

The multiplier performs amplitude modulation, similar to balanced modulation, when a dc term is added to the modulating signal with the Y-offset adjust potentiometer (see Figure 30).

Here, the identity is:

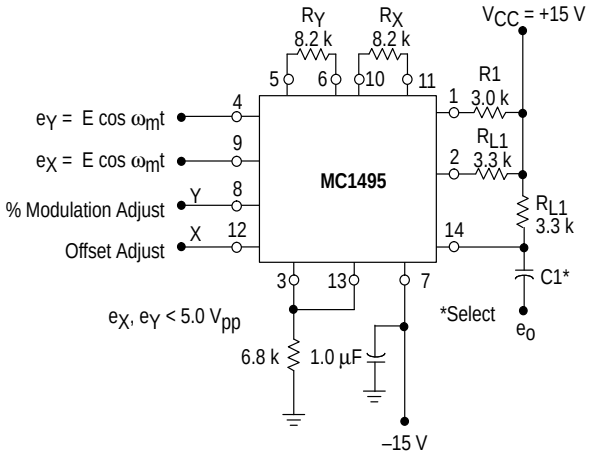
$$E_m(1 + m \cos \omega_m t) E_c \cos \omega_c t = KE_m E_c \cos \omega_c t + \frac{KE_m E_c m}{2} [\cos(\omega_c + \omega_m)t + \cos(\omega_c - \omega_m) t]$$

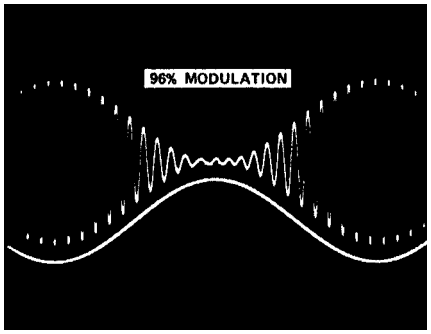
where m indicates the degrees of modulation. Since m is adjustable, via potentiometer P_1, 100% modulation is possible. Without extensive tweaking, 96% modulation may be obtained where ω_c and ω_m are the same as in the balanced modulator example.

Linear Gain Control

To obtain linear gain control, the designer can feed to one of the two MC1495 inputs a signal that will vary the unit's gain. The following example demonstrates the feasibility of this application. Suppose a 200 kHz sinewave, 1.0 V peak-to-peak, is the signal to which a gain control will be added. The dynamic range of the control voltage V_C is 0 V to +1.0 V. These must be ascertained and the proper values of R_X and R_Y can be selected for optimum performance. For the 200 kHz operating frequency, load resistors of 100 Ω were chosen to broaden the operating bandwidth of the multiplier, but gain was sacrificed. It may be made up with an amplifier operating at the appropriate frequency (see Figure 31).

Figure 30. Amplitude Modulation





The signal is applied to the unit's Y-input. Since the total input range is limited to 1.0 V_{pp}, a 2.0 V swing, a current source of 2.0 mA and an R_Y value of 1.0 kΩ is chosen. This takes best advantage of the dynamic range and insures linear operation in the Y-channel.

Since the X-input varies between 0 and +1.0 V, the current source selected was 1.0 mA, and the R_X value chosen was 2.0 kΩ. This also insures linear operation over the X-input dynamic range. Choosing R_L = 100 assures wide bandwidth operation.

Hence, the scale factor for this configuration is:

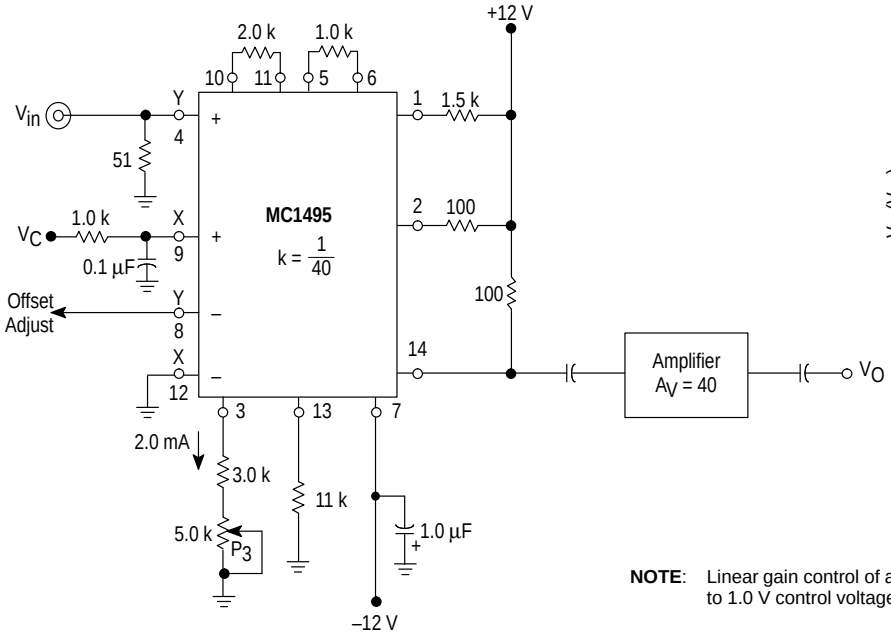
$$K = \frac{R_L}{R_X R_Y I_3}$$

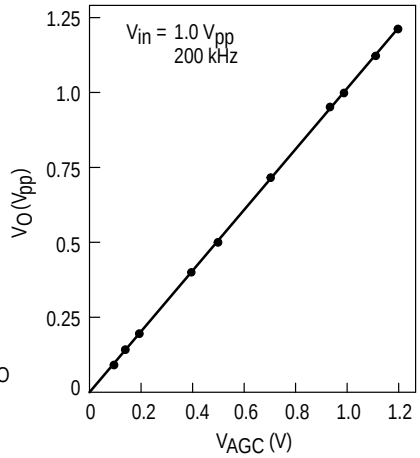
$$= \frac{100}{(2\text{ k})(1\text{ k})(2 \times 10^3)}\ V^{-1}$$

$$= \frac{1}{40}\ V^{-1}$$

The 2 in the numerator of the equation is missing in this scale factor expression because the output is single-ended and ac coupled.

Figure 31. Linear Gain Control

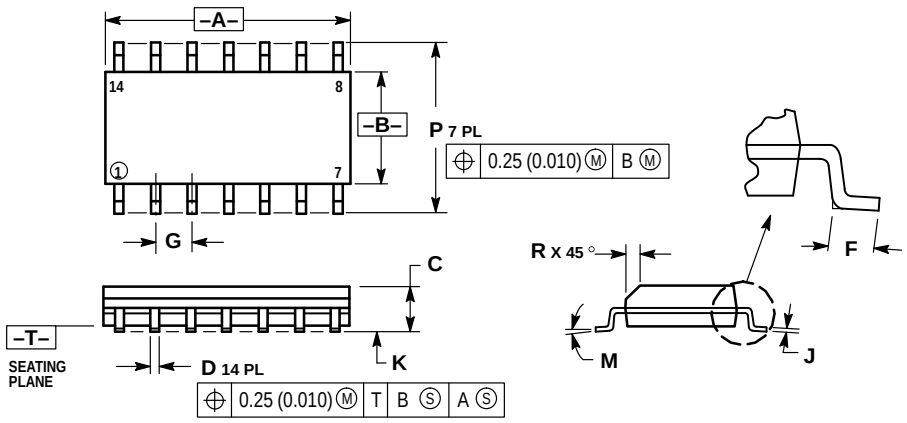




NOTE: Linear gain control of a 1.0 V_{pp} signal is performed with a 0 V to 1.0 V control voltage. If V_C is 0.5 V the output will be 0.5 V_{pp}.

OUTLINE DIMENSIONS

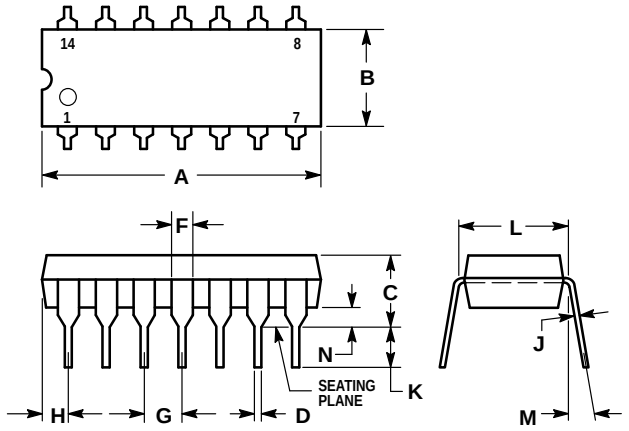
D SUFFIX
PLASTIC PACKAGE
CASE 751A–03
ISSUE F



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

P SUFFIX
PLASTIC PACKAGE
CASE 646–06
ISSUE L



NOTES:
1. LEADS WITHIN 0.13 (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
4. ROUNDED CORNERS OPTIONAL.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.300 BSC		7.62 BSC	
M	0 °	10 °	0 °	10 °
N	0.015	0.039	0.39	1.01

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